CLAIMS

1. A bonded structure comprising:

a first structure;

a second structure; and

a low temperature grown semiconductor bonding layer that bonds the first and second structures.

2. The bonded structure of claim 1, wherein the bonding layer contains at least one of amorphous and polycrystalline semiconductor material.

3. The bonded structure of claim 1, wherein the bonding layer has substantially no preferred orientation with respect to either of the first and second structures.

4. The bonded structure of claim 1, wherein the first and second structures have substantially no preferred orientation with respect to each other.

5. The bonded structure of claim 1, wherein electrical conduction through the bonding layer is essentially independent of orientation of any of the first and second structures and the bonding layer.

6. The bonded structure of claim 1, wherein the bonding layer is substantially optically transparent to light emitted by the bonded structure.

7. The bonded structure of claim 1, wherein the bonding produced by the bonding layer is strong enough to be substantially unaffected by processing of the bonded structure.

8. The bonded structure of claim 1, wherein the bonding produced by the bonding layer is strong enough to be substantially unaffected by annealing temperatures coupled with annealing times used during regrowth of semiconductor.

9. The bonded structure of claim 1, wherein at least one of the first and second structures comprises a semiconductor substrate.

10. The bonded structure of claim 1, wherein at least one of the first and second structures comprises a non-semiconductor substrate.

11. The bonded structure of claim 1, wherein the bonding layer has a thickness of about 3 nm to about 600 nm.

12. The bonded structure of claim 1, wherein the bonding layer comprises at least one of low temperature grown (Ga,As), (Ga,P), and (Ga,N).

13. The bonded structure of claim 1, wherein the bonding layer is electrically conductive over a range of voltages used during operation of a device that contains the bonded structure.

14. The bonded structure of claim 1, wherein the bonding layer comprises at least one compound semiconductor.

15. The bonded structure of claim 14, wherein the compound semiconductor comprises Si as a dopant.

16. The bonded structure of claim 14, wherein the compound semiconductor comprises a dopant that helps to control morphology of the low-temperature grown compound semiconductor.

17. The bonded structure of claim 1, wherein the bonding layer is strong enough to be substantially unaffected by use of the bonded structure in a user application.

18. The bonded structure of claim 1, wherein the bonding layer comprises a Ga-rich low temperature semiconductor.

19. A photodiode comprising the bonded structure of claim 1.

20. A transistor comprising the bonded structure of claim 1.

21. A heterojunction bipolar transistor comprising the bonded structure of claim 1.

22. A high-electron-mobility transistor comprising the bonded structure of claim 1.

23. A light-emitting diode comprising the bonded structure of claim 1.

24. A laser comprising the bonded structure of claim 1.

25. The bonded structure of claim 1, wherein at least one of the first and second structures comprises a semi-insulating substrate.

26. The bonded structure of claim 1, wherein at least one of the first and second structures comprises an insulator.

27. The bonded structure of claim 1, wherein at least one of the first and second structures comprises a pseudomorphic structure.

28. The bonded structure of claim 1, wherein at least one of the first and second structures comprises a multiple quantum well structure.

29. The bonded structure of claim 1, wherein the bonding layer is devoid of polymers, ceramics, and metals.

30. A method of bonding two structures together, the method comprising:

depositing low temperature grown semiconductor bonding layers on first and second structures to form a combined structure;

placing the bonding layers in contact with each other;

applying pressure to the combined structure; and

annealing the combined structure under conditions sufficient for the bonding layers to bond the first and second structures together.

31. The method of claim 30, further comprising applying the pressure substantially uniformly to the combined structure during annealing.

32. The method of claim 30, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material.

33. The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,As) and the annealing of the combined structure occurs at a temperature of between about 300°C and 500°C and for a time sufficient for the bonding layers to form a (Ga,As) material that is substantially entirely polycrystalline.

34. The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,P) and the annealing of the combined structure occurs at a temperature of between about 500°C and 700°C and for a time sufficient for the bonding layers to form a (Ga,P) material that is substantially entirely polycrystalline.

35. The method of claim 30, wherein the bonding layer comprises at least one of amorphous and polycrystalline (Ga,N) and the annealing of the combined structure occurs at a temperature of between about 700°C and 900°C and for a time sufficient for the bonding layers to form a (Ga,N) material that is substantially entirely polycrystalline.

36. The method of claim 30, wherein the bonding layers are placed in contact with each other without regard for a relative angular orientation of the first and second structures to each other.

37. The method of claim 30, wherein at least one of the first and second structures comprises a non-semiconductor substrate.

38. The method of claim 30, further comprising fabricating at least one of an electronic and optoelectronic device from the combined structure.

39. The method of claim 30, wherein the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong enough to survive subsequent processing at temperatures higher than that used during the bonding.

40. The method of claim 30, wherein a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure.

41. The method of claim 30, wherein a bonding interface produced by the annealing is strong enough to be substantially unaffected by processing of the combined structure.

42. The method of claim 30, wherein the deposition deposits between about 3 nm and about 600 nm of material on each of the first and second structures.

43. The method of claim 30, wherein the deposition deposits at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) on at least one of the first and second structures.

44. The method of claim 30, further comprising selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures.

45. The method of claim 44, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer.

46. The method of claim 30, further comprising selecting a composition of the bonding layer such that a polycrystalline semiconductor layer is deposited on at least one of the first and second structures.

47. The method of claim 46, wherein the annealing of the combined structure occurs under conditions sufficient for the bonding layers to recrystallize into a polycrystalline material.

48. The method of claim 30, wherein the annealing occurs at temperatures of at most about 800°C.

49. The method of claim 30, wherein the bonding layer comprises a compound semiconductor.

50. The method of claim 49, further comprising doping the bonding layer with Si.

51. The method of claim 49, further comprising doping the bonding layer with a dopant that helps to control morphology of the compound semiconductor.

52. The method of claim 30, wherein Ga-rich low temperature grown semiconductor bonding layers are deposited.

53. The method of claim 30, the bonding layer is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100°C.

54. A bonded structure comprising:

a first structure;

a second structure; and

a low temperature grown compound semiconductor bonding layer that bonds the first and second structures and contains at least one of amorphous and polycrystalline semiconductor material.

55. The bonded structure of claim 54, wherein the first and second structures have substantially no preferred orientation with respect to each other.

56. The bonded structure of claim 54, wherein electrical conduction through the bonding layer is essentially independent of orientation of any of the first and second structures and the bonding layer.

57. The bonded structure of claim 54, wherein the bonding layer is substantially optically transparent to light emitted by the bonded structure.

58. The bonded structure of claim 54, wherein the bonding produced by the bonding layer is strong enough to be substantially unaffected by processing of the bonded structure.

59. The bonded structure of claim 54, wherein the bonding produced by the bonding layer is strong enough to be substantially unaffected by annealing temperatures coupled with annealing times used during regrowth of semiconductor.

60. The bonded structure of claim 54, wherein at least one of the first and second structures comprises a semiconductor substrate.

61. The bonded structure of claim 54, wherein at least one of the first and second structures comprises a non-semiconductor substrate.

62. The bonded structure of claim 54, wherein the bonding layer has a thickness of about 3 nm to about 600 nm.

63. The bonded structure of claim 54, wherein the bonding layer comprises at least one of low temperature grown (Ga,As), (Ga,P), and (Ga,N).

64. The bonded structure of claim 54, wherein the compound semiconductor comprises Si as a dopant.

65. The bonded structure of claim 54, wherein the compound semiconductor comprises a dopant that helps to control morphology of the compound semiconductor.

66. The bonded structure of claim 54, wherein the bonding layer is strong enough to be substantially unaffected by use of the bonded structure in a user application.

67. The bonded structure of claim 54, wherein at least one of the first and second structures comprises a semi-insulating substrate.

68. The bonded structure of claim 54, wherein at least one of the first and second structures comprises a pseudomorphic structure.

69. The bonded structure of claim 54, wherein at least one of the first and second structures comprises a multiple quantum well structure.

70. The bonded structure of claim 54, wherein the bonding layer is devoid of polymers, ceramics, and metals.

71. The bonded structure of claim 54, wherein the compound semiconductor comprises a Ga-rich semiconductor bonding layer.